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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/822,063	03/30/2001	James E. O'Toole	MI40-325	9960

21567 7590 03/30/2004

WELLS ST. JOHN P.S.
601 W. FIRST AVENUE, SUITE 1300
SPOKANE, WA 99201

EXAMINER	
HOLLOWAY III, EDWIN C	
ART UNIT	**PAPER NUMBER**
2635	11

DATE MAILED: 03/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/822,063	O'TOOLE ET AL.	
	Examiner	Art Unit	
	Edwin C. Holloway, III	2635	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 March 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *253-284* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *253-284* is/are rejected.

7)☒ Claim(s) *258-259* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4-7,9-10*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

EXAMINER'S RESPONSE

1. In response to the application filed 3-30-01, the preliminary amendment filed 3-30-01 has been entered and the application has been examined. The examiner has considered the presentation of claims in view of the disclosure and the present state of the prior art. And it is the examiner's opinion that the claims are unpatentable for the reasons set forth in this Office action:

SPECIFICATION

2. Applicant is reminded to continue updating the specification to include the current status of the various incorporated applications to indicate if they are abandoned or allowed and to include any Patents numbers or continuing serial numbers. For example, identification of patent number 6466634 should be included with the reference to serial number 09161512 in the continuing data. Applicant is required to maintain a clear line of demarcation between the claims of the instant application and those of the incorporated applications.

Claim Objections

3. Claims 258-259 are objected to because of the following informalities: Claim 258 refers to "claim 253, wherein the charge pump comprises," but claim 253 does not include a charge

pump. Should claim 258 depend from claim 254?. Appropriate correction is required.

Double Patenting

4. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5. Claims 253-284 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-30 of U.S. Patent No. 6466634B1. Although the conflicting claims are not identical, they are not patentably distinct from each other because claims 253-284 are generally broader than the clams in your patent. Broader claims in a later application constitute obvious double patenting of narrow claims in an issued patent. See *In re Van Ornum and Stang*, 214, USPQ 761, 766, and 767 (CCPA) (the court sustained an obvious double patenting rejection of generic claims in a

continuation application over narrower species claims in an issued patent); *In re Vogel*, 164 USPQ 619, 622, and 623 (CCPA 1970) (generic application claim specifying "meat" is obvious double patenting of narrow patent claim specifying "pork").

Claim Rejections - 35 USC § 102 & 103

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

9. Claim 253 is rejected under 35 U.S.C. 102([]) as being anticipated by Partyka (US 5121407).

Partyka discloses a communication system with a transmitter circuitry having a phase locked loop (PLL) 100 outputting a carrier 111 including a voltage controlled oscillator (VCO) 110, to multiply the frequency of a digital clock 124 by a multiple M and control circuitry 120 to maintain a frequency. The circuitry includes a divider 122 to divide the multiplied frequency by M. See fig. 1 and col. 6 lines 1-49 and col. 8 lines 58-66.

10. Claim 253-255, 260, 263, 266-269, 272-273 and 280-282 are rejected under 35 U.S.C. 103(a) as being unpatentable over Partyka (US 5121407) as applied above and Sutardja (5576647).

Partyka was discussed above.

Sutardja discloses an CMOS PLL with quadrature output that can function as a frequency synthesizer desirable for use in analogous art RF communications. The PLL includes phase detector 110 connected to a charge pump 120 to a passive loop filter 124 to a voltage controlled oscillator 128 to a counter/divider 130 back to the phase detector 110. The counter 106 may be eliminated in which case the reference signal REF is input directly to the phase detector and the PLL would provide

an output CLKOUT of the reference REF multiplied by the predetermined number of the counter/divider 130 to provide the desired output frequency. This circuit is very similar to that of Irwin, discussed below, with the addition of being a monolithic CMOS PLL with a quadrature VCO. See fig. 2, col. 2 lines 31-54, col. 3 lines 36-67 and col. 4 line 54 - col. 5 line 21.

Regarding claim 253, CMOS integrated circuit (IC) was not given weight in the rejection made above because it was only in the preamble. If CMOS IC is given weight, then it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included the CMOS IC PLL of Sutardja in the transmitter of Partyka in order to provide advantages such as low power, low cost, high operating frequency, low jitter. The combination is suggested by Partyka disclosing an RF transmitter PLL with IC's in col. 6 line 33 and Sutardja discloses a PLL with quadrature outputs for RF applications in col. 2 line 17 and col. 3 line 60.

Regarding claim 254, Partyka includes phase detector 120 and loop filter 118. Partyka lacks a charge pump, but Sutardja discloses a charge pump for a PLL. See the title. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have include the charge pump of

Sutardja in the combination applied above for the reasons applied above and because the charge pump of Sutardja includes advantages such as accurate operation at very low current and high frequency in col. 2 lines 14-21.

Regarding claim 255, Partyka lacks plural VCO outputs separate by phase, but Sutardja discloses a VCO with in-phase and quadrature outputs (separated by 90 degrees) for RF applications. See the abstract col. 1 line 50, col. 2 line 17 and col. 9 line 20. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have include the in-phase and quadrature VCO outputs of Sutardja in the combination applied above for the reasons applied above and because the quadrature output would have been useful with the RF transmitter of Partyka such as for quadrature modulation.

Claim 260 includes a modulator in addition to the limitations recited in claim 255. Partyka includes a modulator 112 in col. 6 line 47. Therefore, claim 260 is rejected for the same reasons applied above to claim 255.

Claim 263 adds to claim 260 limitations corresponding to claim 254. Therefore, claim 263 is rejected for the same reasons applied above to claim 254 and 255.

Claim 266 corresponds to claim 253 with the addition of the control circuit providing comparison and pump up/down to a

charge pump. These additions are provided by the phase detector 110 and charge pump 120 in fig. 1 of Sutardja and would have been obvious for the reasons applied above to claim 254.

Regarding claims 267-268 the loop filter and charge pump would have been obvious for the same reasons applied to claim 254.

Regarding claim 269, Partyka discloses a binary divider or modulus prescaler 122 that divides by the predetermined multiple M. The choice of M in example described in col. 16 is M=128=16x8. Therefore the predetermined multiple M at least comprises 16. Further, dividing by only 16 would have been obvious because any power of two (M=2, 4, 8, 16, 32, 64, 128, 256, 512, 1024, etc.) may have been chosen as long a multiplying the reference frequency from the reference oscillator by the value of M would produce the desired carrier frequency.

Claim 272 corresponds to claim 266 with the addition of the limitations of claim 255. Therefore, claim 272 is rejected for the same reasons applied above to claim 266 and 255.

Regarding claim 273, Partyka discloses a binary divider or modulus prescaler 122 that divides by the predetermined multiple M. The choice of M in example described in col. 16 is M=128=16x8. Therefore the predetermined multiple M at least comprises 16. Further, dividing by only 16 would have been

obvious because any power of two (M=2, 4, 8, 16, 32, 64, 128, 256, 512, 1024, etc.) may have been chosen as long a multiplying the reference frequency from the reference oscillator by the value of M would produce the desired carrier frequency.

Claim 280 corresponds to claim 266 with the addition of the limitations of claim 260. Therefore, claim 280 is rejected for the same reasons applied above to claim 266 and 260.

Regarding claims 281 the VCO of Sutardja includes transistor stages in figs. 4-17. If variable resistance is not clear in these figures, then please not the variable resistance 308 in fig. 3. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have to have included these in the combination applied above for advantages such as reducing jitter.

Regarding claim 282 the loop filter and phase-frequency detector would have been obvious for the same reasons applied to claim 254.

11. Claim 256-257, 274-277 are rejected under 35 U.S.C. 103(a) as being unpatentable over Partyka (US 5121407) and Sutardja (5576647) as applied above and further in view of Nystrom (US 5412351).

Regarding claims 256-257, 274-277, Partyka includes a

multiplier 112 for modulation, but does not specify Gilbert cells.

Applicant admits on pages 208-210 that four quadrant Gilbert cell multipliers and CMOS Gilbert cell doublers are well known.

Nystrom discloses a quadrature oscillator network with multiple oscillator inputs separated by phase and input to a plurality of connected Gilbert cells. See fig. 8 and col. 10.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have included the Gilbert cell multipliers/doublers of claims 256-257, 274-277 in the combination applied above because Nystrom discloses these for quadrature modulation that is suggested by the multiplier functioning as a modulator in Partyka. Further, CMOS doublers would have been obvious because the admitted prior art includes CMOS Gilbert cell doublers which would have provided the advantages of an all CMOS transmitter such as reduced power and simpler manufacturing suggested by the inclusion of CMOS in Sutardja. The inclusion of phase angle spaced inputs to the doublers would have been obvious in view of the four quadrants in the admitted prior art or multiple phase inputs in Nystrom in order to provide quadrature or symmetrical operation.

12. Claim 258-259, 264-265, 270-271, 278-279 and 283-384 are rejected under 35 U.S.C. 103(a) as being unpatentable over Partyka (US 5121407) and Sutardja (5576647) as applied above and further in view of Hogeboom (US 5334951).

The above applied prior art includes all the claimed limitations except for the two charge pumps controlled with different steps.

Hogeboom discloses a PLL with two charge pumps (230, 230') controlled for coarse and fine adjustment steps. See fig. 7 and cols. 8-9 and the abstract.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have included in the combination applied above the two charge pumps controlled in different steps such as the coarse and fine adjustments disclosed in Hogeboom for more stable and predictable performance.

13. Claim 261-262 are is rejected under 35 U.S.C. 103(a) as being unpatentable over Partyka (US 5121407) and Sutardja (5576647) as applied above and further in view of Necoechea (US 5191295).

Necoechea discloses a phase shift vernier with a PLL as in applicant's invention including a VCO with 8 phase outputs for

quadrature modulation. See fig. 3 and col. 4 line 43 - col. 6 line 11.

Regarding claim 261, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included the VCO with 8 phase outputs in the PLL of the combination applied above in order to provide outputs for quadrature modulation.

Regarding claim 262, Partyka discloses a binary divider or modulus prescaler 122 that divides by the predetermined multiple M. The choice of M in example described in col. 16 is M=128=16x8. Therefore the predetermined multiple M at least comprises 16. Further, dividing by only 16 would have been obvious because any power of two (M=2, 4, 8, 16, 32, 64, 128, 256, 512, 1024, etc.) may have been chosen as long a multiplying the reference frequency from the reference oscillator by the value of M would produce the desired carrier frequency.

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Linder (US 3694776), Schaible (US 3921094)and Jeong (US 5705947) disclose PLL circuits.

CONTACT INFORMATION

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any inquiry of a general nature should be directed to the Technology Center 2600 receptionist at (703) 305-4700 or TC 2600 Customer Service at (703) 306-0377.

Facsimile submissions may be sent via fax number (703) 872-9306 to customer service for entry by technical support staff. Questions regarding fax submissions should be directed to customer service voice line (703) 306-0377.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Edwin C. Holloway, III whose telephone number is (703) 305-4818. The examiner can normally be reached on M-F (8:30-5:00). If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Horabik can be reached on (703) 305-4704.

EH
3/20/04

EDWIN C. HOLLOWAY, III
PRIMARY EXAMINER
ART UNIT 2635